What is claimed is:

1. A control thin film transistor for controlling an organic light-emitting diode (OLED), comprising:

a substrate;

a semiconductor layer disposed on the substrate as a channel region;

a first and second doped region sequentially disposed on a first side of the semiconductor layer, wherein the doped concentration of the first doped region is lower than that of the second doped region, and the first doped region serves as a single-side lightly doped drain region and the second doped region serves as a drain region;

a third doped region disposed on a second side of the semiconductor layer, which is opposite to the first side, serving as a source region;

an insulating layer disposed on the surface of the semiconductor layer, and the first, second, and third regions;

a source and drain electrode penetrating the insulating layer contacting the source and drain regions respectively, wherein the drain electrode receives a drain voltage and the source electrode is electrically connected to an OLED unit; and

a conductive layer serving as a gate layer disposed in the insulating layer, at approximately the top right portion of the semiconductor layer.

2. The control thin film transistor as claimed in claim 1, wherein the semiconductor layer is composed of polysilicon.

3. The control thin film transistor as claimed in claim 1, wherein the first, second and third doped regions are n-type doped.

4. The control thin film transistor as claimed in claim 1, wherein the first, second and third doped regions are p-type doped.

5. The control thin film transistor as claimed in claim 1, wherein the first, second and third doped regions are mainly composed of silicon.

6. A control thin film transistor for controlling an organic light-emitting diode (OLED), comprising:

a substrate;

a semiconductor layer disposed on the substrate as a channel region;

a first and second doped region sequentially disposed on a first side of the semiconductor layer, wherein the doped concentration of the first doped region is lower than that of the second doped region, and the second doped region serves as a drain region;

a third and fourth doped region sequentially disposed on a second side of the semiconductor layer, which is opposite to the first side; wherein the doped concentration of the third

doped region is lower than that of the fourth doped region that serves as a source region and the length of the third doped region is less than that of the first doped region;

an insulating layer disposed on the surface of the semiconductor layer, and the first, second, third and fourth regions;

a source and drain electrode penetrating the insulating layer contacting the source and drain regions respectively, wherein the drain electrode receives a drain voltage and the source electrode is electrically connected to an OLED unit; and

a conductive layer serving as a gate layer disposed in the insulating layer, at approximately the top right portion of the semiconductor layer.

7. The control thin film transistor as claimed in claim 6, wherein the semiconductor layer is composed of polysilicon.

8. The control thin film transistor as claimed in claim 6, wherein the first, second, third and fourth doped regions are n-type doped.

9. The control thin film transistor as claimed in claim 6, wherein the first, second, third and fourth doped regions are p-type doped.

10. The control thin film transistor as claimed in claim 6, wherein the first, second, third and fourth doped regions are mainly composed of silicon.

11. An electroluminescent display device, which sequentially scans a plurality of pixels composing a display screen and provides current to the scanned pixels according to pixel signals received while scanning, thereby activating electroluminescent units in the pixels to display figures on the display screen according to the pixel signals, the device is characterized by having a plurality of control TFTs as claimed in claim 1 in the pixels to control the current provided to the scanned pixels.

12. An electroluminescent display device, which sequentially scans a plurality of pixels composing a display screen and provides current to the scanned pixels according to pixel signals received while scanning, thereby activating electroluminescent units in the pixels to display figures on the display screen according to the pixel signals, the device is characterized by having plurality of control TFTs as claimed in claim 5 in the pixels to control the current provided to the scanned pixels.

13. A method of fabricating a control thin film transistor for controlling a current of an OLED unit, comprising the steps of:

providing a substrate;

forming and defining a semiconductor layer on the substrate;

forming a first photoresist layer covering a portion of the semiconductor layer, exposing

predetermined portions on the semiconductor layer for a source and drain regions;

performing a first ion implantation of the semiconductor layer using the first photoresist layer as a mask to form the source and drain regions thereon;

removal of the first photoresist layer;

forming a first insulating layer covering the surface of the substrate and the semiconductor layer;

forming a second photoresist layer on the first insulating layer, which covers the un-implanted area of the semiconductor layer but exposes only a portion of the un-implanted area of the semiconductor layer adjacent to the drain region;

performing a second ion implantation of the semiconductor layer using the second photoresist layer as a mask to form a lightly doped region with a doped concentration lower than that of the adjacent drain region;

removal of the second photoresist layer;

forming a gate layer on the first insulating layer and at approximately the right top of the un-doped semiconductor layer;

forming a second insulating layer covering the surface of the first insulating layer and the gate layer; and

forming a source and drain electrodes penetrating the first and second insulating layer in

contact with the source and drain regions respectively, wherein the drain electrode receives a drain voltage and the source electrode is electrically connected to an OLED unit.

14. The method as claimed in claim 13, wherein forming the semiconductor layer further comprises the steps of:

forming an amorphous silicon layer on the substrate; and

performing a laser treatment of the amorphous silicon layer to crystallize as a polysilicon layer as the semiconductor layer.

15. The method as claimed in claim 14, wherein dopants of the first and second ion implantation are n-type dopants.

16. The method as claimed in claim 14, wherein dopants of the first and second ion implantation are p-type dopants.

17. The method as claimed in claim 14, wherein the first and second insulating layers are silicon oxide.

18. A method of fabricating a control thin film transistor for controlling a current of an OLED unit, comprising the steps of:

providing a substrate;

forming and defining a semiconductor layer on the substrate;

forming a first photoresist layer covering a portion of the semiconductor layer, exposing predetermined portions on the semiconductor layer for a source and drain region;

performing a first ion implantation of the semiconductor layer using the first photoresist layer as a mask to form the source and drain regions thereon;

removal of the first photoresist layer;

forming a first insulating layer covering the surface of the substrate and the semiconductor layer;

forming a second photoresist layer on the first insulating layer, which covers the un-implanted area of the semiconductor layer but exposes two portions of the un-implanted area of the semiconductor layer adjacent to the drain and source regions respectively, wherein the portion adjacent to the drain region is greater than the portion adjacent to the source region;

performing a second ion implantation of the semiconductor layer using the second photoresist layer as a mask to form lightly doped drain and source regions with a dopant concentration lower than that of the adjacent drain and source regions respectively, wherein the lightly doped drain region is larger than the lightly doped source region;

removal of the second photoresist layer;

forming a gate layer on the first insulating layer and at approximately the right top of the un-doped semiconductor layer;

forming a second insulating layer covering the surface of the first insulating layer and the gate layer; and

forming a source and drain electrodes penetrating the first and second insulating layer in contact with the source and drain regions respectively, wherein the drain electrode receives a drain voltage and the source electrode is electrically connected to an OLED unit.

19. The method as claimed in claim 18, wherein forming the semiconductor layer further comprises the steps of:

forming an amorphous silicon layer on the substrate; and

performing a laser treatment of the amorphous silicon layer to crystallize as a polysilicon layer as the semiconductor layer.

20. The method as claimed in claim 19, wherein dopants of the first and second ion implantation are n-type dopants.

21. The method as claimed in claim 19, wherein dopants of the first and second ion implantation are p-type dopants.

22. The method as claimed in claim 19, wherein the first and second insulating layers are silicon oxide.